Certificate / Certificat

Zertifikat / 合格証

FRS 091023 C001

exida hereby confirms that the:

DeltaV SIS Smart Logic Solver
(including SLS Terminal Block or
SLS Redundant Terminal Block)

Fisher Rosemount Systems, Inc.
(an Emerson Automation Solutions company)
Round Rock, TX USA

has been assessed per the relevant requirements of:

IEC 61508 : 2010 Parts 1-7

NFPA 72, EN54-2 Logic Solver

and meets requirements providing a level of integrity to:

Systematic Capability: SC 3 (SIL 3 Capable)

Random Capability: Type B Element

SIL 3 @ HFT = 0; Route 1_H

PFH/PFD_{AVG} and Architecture Constraints must be verified for each application

Safety Function:
The DeltaV SIS will perform the configured safety logic and execute the automatic diagnostics in the specified time period.

Application Restrictions:
The unit must be properly designed into a Safety Instrumented Function per the Safety Manual requirements.

John C Yozallinas
Evaluating Assessor

Certifying Assessor

The manufacturer may use the mark:

Revision 3.1 March 11, 2021
Surveillance Audit Due
February 1, 2024

ANSI National Accreditation Board
ACCREDITED
ISO/IEC 17065
PRODUCT CERTIFICATION BODY
#1004

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Systematic Capability: SC 3 (SIL 3 Capable)

Random Capability: Type B Element

SIL 3 @ HFT = 0; Route 1_H

PFH/PFD_{AVG} and Architecture Constraints must be verified for each application

DeltaV SIS Smart Logic Solver

Systematic Capability:

The product has met manufacturer design process requirements of Safety Integrity Level (SIL) 3. These are intended to achieve sufficient integrity against systematic errors of design by the manufacturer.

A Safety Instrumented Function (SIF) designed with this product must not be used at a SIL level higher than stated.

Random Capability:

The SIL limit imposed by the Architectural Constraints must be met for each element.

IEC 61508 Failure Rates in FIT*

Failure Categories	λ_{SD}	λ_{SU}	λ_{DD}	λ_{DU}
Common (DET)	1343	11	932	3
Common (ET)	1091	3	1251	4
AI Channel	31	0	20	0.006
DI Channel	39	2	13	0
AO Channel	31	0	20	0.006
DO Channel (DET)	21	0.3	10	0
DO Channel (ET)	16	0	17	0.3

* FIT = 1 failure / 10^9 hours

SIL Verification:

The Safety Integrity Level (SIL) of an entire Safety Instrumented Function (SIF) must be verified via a calculation of PFH/PFD_{avg} considering redundant architectures, proof test interval, proof test effectiveness, any automatic diagnostics, average repair time and the specific failure rates of all products included in the SIF. Each element must be checked to assure compliance with minimum hardware fault tolerance (HFT) requirements.

The following documents are a mandatory part of certification:

Assessment Report: FRS 09-10-23 R001 V3 R1 (or later)

Safety Manual: D800032X012

80 N Main St
Sellersville, PA 18960